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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,980	10/03/2003	Salvador Salcido JR.	10030277-1	1555

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EXAMINER
TRAN, LONG K

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/678,980	SALCIDO ET AL.
	Examiner	**Art Unit**
	Long K. Tran	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 07, 2005 has been entered.

Claim Objections

2. Claims **1** and **22** are objected to because of the following informalities:

Claim 1, line 5, change “the layer” to –the interconnection layer--;

Claim 22, line 4: delete “and’ at the end of the line.

Appropriate correction is required;

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1 – 8** and **12 – 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Der Have (US Patent no. 5,128,737).

5. Regarding claim **1,** Van Der Have discloses an integrated circuit assembly comprising:

a substrate 57/45 (fig. 12) of semiconductor material including a circuit integrally 45 (column 28, lines 1 6) formed therein;

an interconnection layer 46 (fig. 12) for carrying a signal to and from a portion of the circuit, the interconnection overlying the substrate and making selective electrical connection to the circuit integrally formed in the substrate, the interconnection layer formed of a first conductive material; and

a distribution layer 47 (fig. 12; **not 48** as argued by the Applicants) overlying the interconnection layer 46, the distribution layer 47 including wire bonding pads 52 (fig. 12; col. 27, lines 12 - 25) for wire bonding to selected electrical signals and distribution grids for distributing a signal over a region of the connection layer, the distribution grids connected to the wire bonding pads and extending over the interconnection, the distribution layer 47 being formed of a second conductive material; and

a plurality of connecting channels 50 (fig. 12; col. 26, lines 64 – 68) connecting selected ones of the distribution grids to selected locations of the interconnection layer.

Van Der Have further discloses the interconnection layer 46 and the distribution layer 47 are formed of metals taken from the group consisting of aluminum, copper and gold (column 26, lines 57 – 65 and claims 1 and 4) but does not explicitly teach the interconnection layer 46 and the distribution layer 47 are made from material different from each other as claimed invention.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select any material from aluminum, copper and gold for the connection layer (copper) and the distribution layer (aluminum) as disclosed by Van Der Have. As the result, the material (copper) of the interconnection layer is different from the material (aluminum) of the distribution layer as claimed invention.

Additionally, the Applicant has presented no discussion in the specification which convinces the Examiner that the particular materials of the interconnection layer and the distribution layer are anything more than one of numerous materials (also disclosed by Van Der Have) a person of ordinary skill in the art would find obvious for the purpose of providing the interconnection layer and the distribution layer. It appears that these changes produce no functional differences and therefore would have been obvious.

Regarding claim **2,** Van Der Have discloses the first conductive material is copper (column 26, lines 57 – 65 and claims 1 and 4).

Regarding claims **3** and **4,** Van Der Have discloses the second conductive material is aluminum (column 26, lines 57 – 65 and claims 1 and 4).

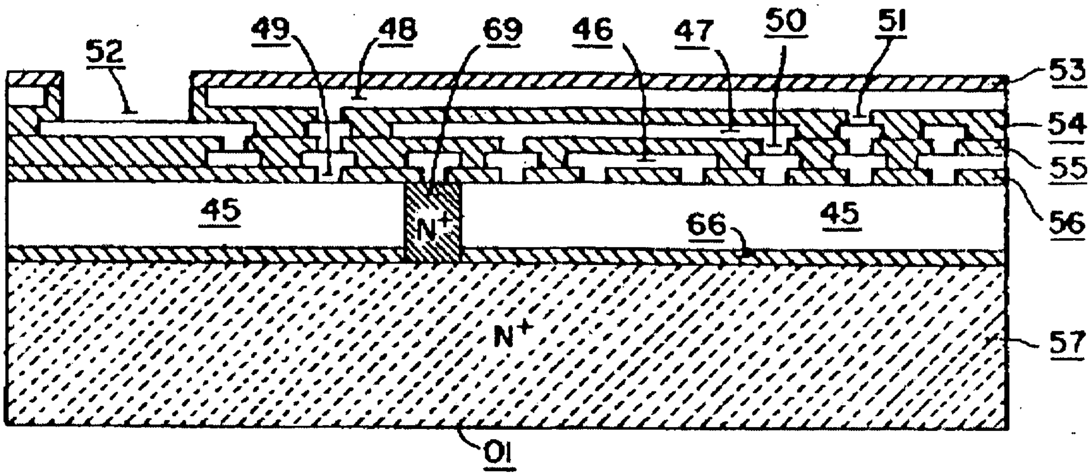

FIGURE 12

Regarding claim **5,** Van Der Have discloses the connecting channels 50 (fig. 12; column 26, lines 64 – 66) are vias.

Regarding claim **6,** Van Der Have discloses the selected locations of interconnection layer 46 include power connections and wherein at least one of the wire bond pads is coupled to the power connections (column 27, lines 33 + and column 34, lines 1 – 29).

Regarding claim **7,** Van Der Have discloses the selected locations of interconnection layer 46 include ground connections and wherein at least one of the wire bond pads is coupled to the ground connections (column 27, lines 33 + and column 34, lines 1 – 29).

Regarding claim **8,** Van Der Have discloses the connecting channels 49 and 50 are distributed throughout the distribution layer (fig. 12).

Regarding claim **12**, Van Der Have discloses the distribution grids form an orthogonal grid pattern (figs. 1 – 8).

Regarding claim **13**, Van Der Have discloses an integrated circuit comprising:

a substrate 45/57 (fig. 12) of semiconductor material and formed of a first metal;

a first metalization layer 46 (fig. 12) overlying the substrate and operable to carry a signal to and from a portion of the circuit and formed of a first metal;

an insulator layer 55 (fig. 12) overlying the metalization layer and including a plurality of vias 50 (fig. 12; col. 26, lines 64 – 68);

a second metalization layer 47 (fig. 12; **not 48** as argued by the Applicants) overlying the insulator layer, and making selective contact with the first metalization layer through the vias 49, 50 (fig. 12; col. 26, lines 64 – 68), the second layer including wire bonding pads 52 (fig. 12; col. 27, lines 12 - 25) and distribution grids (figs. 1 – 8) coupled bonding pads and distributed over the insulator layer, each distribution grid operable to distribute a signal.

Van Der Have further discloses the interconnection layer 46 and the distribution layer 47 are formed of metals taken from the group consisting of aluminum, copper and gold (column 26, lines 57 – 65 and claims 1 and 4) but does not explicitly teach the interconnection layer 46 and the distribution layer 47 are made from material different from each other as claimed invention.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select any material from aluminum, copper and gold for the connection layer (copper) and the distribution layer (aluminum) as disclosed by Van

Der Have. As the result, the material (copper) of the interconnection layer is different from the material (aluminum) of the distribution layer as claimed invention.

Additionally, the Applicant has presented no discussion in the specification which convinces the Examiner that the particular materials of the interconnection layer and the distribution layer are anything more than one of numerous materials (also disclosed by Van Der Have) a person of ordinary skill in the art would find obvious for the purpose of providing the interconnection layer and the distribution layer. It appears that these changes produce no functional differences and therefore would have been obvious.

Regarding claim **14,** Van Der Have discloses the first conductive material is copper (column 26, lines 57 – 65 and claims 1 and 4).

Regarding claims **15** and **16,** Van Der Have discloses the second conductive material is aluminum (column 26, lines 57 – 65 and claims 1 and 4).

Regarding claim **17,** Van Der Have discloses the connecting channels 50 (fig. 12; column 26, lines 64 – 66) are vias.

6. Claims **9**, **10, 11, 18**, **20, 21** and **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Der Have in view of Lee (US Patent Application Publication no. 2004/0023436).

7. Regarding claim **9**, Van Der Have discloses the claimed invention of claim 1 and shows bond pad window 52 allowing the interconnect layer 46 and the distribution layer 47 exposed for wire-bonding for the purpose of electrical conductive connection of I/O

to a circuit external. Van Der Have does not teach a package having a surface wire bonding pads for coupling to the wire bonding pads of the distribution layer.

However, it is known and also shown by Lee that an IC die substrate 62 (fig. 12) is connected to a package support 60 ([0015] and [0017]). It would have been obvious to one ordinary skill in the art at the time the invention was made to provide wire bonds coupling wire bonding pads of the package to wire bonding pads of the distribution layer in order to complete forming a semiconductor device.

Regarding claim **10**, Van Der Have discloses the wire bonding pads of the package include ground and power pads (not, shown; column 33 lines 1+ and column 34 lines 1+)

Regarding claim **11**, Van Der Have discloses the claimed invention of claim 1 except for the wire bonding pads are disposed at the periphery of the distribution layer.

However, figure 12 of Lee illustrates wire bonding 25 connected the layers of interconnect metal (note: including a second metalization layer as claimed) of IC die substrate 62 to the package supporting 60 ([0015] and [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the bonding pads of Van Der Have to the locations as shown by Lee, in order to mount more than one IC die inside the package ([0016]).

Regarding claim **18**, Van Der Have discloses the claimed invention of claim 13 and shows bond pad window 52 allowing the interconnect layer 46 and the distribution layer 47 exposed for wire-bonding for the purpose of electrical conductive connection of

I/O to a circuit external. Van Der Have does not teach a package having a surface wire bonding pads for coupling to the wire bonding pads of the distribution layer.

However, it is known and also shown by Lee that an IC die substrate 62 (fig. 12) is connected to a package support 60 ([0015] and [0017]). It would have been obvious to one ordinary skill in the art at the time the invention was made to provide wire bonds coupling wire bonding pads of the package to wire bonding pads of the distribution layer in order to complete forming a semiconductor device.

Regarding claim **19**, Van Der Have discloses the wire bonding pads of the package include ground and power pads (not, shown; column 33 lines 1+ and column 34 lines 1+)

Regarding claim **20**,Van Der Have discloses the claimed invention of claim 13 except for the wire bonding pads are disposed at the periphery of the distribution layer.

However, figure 12 of Lee illustrates wire bonding 25 connected the layers of interconnect metal (note: including a second metalization layer as claimed) of IC die substrate 62 to the package supporting 60 ([0015] and [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the bonding pads of Van Der Have to the locations as shown by Lee, in order to mount more than one IC die inside the package ([0016]).

Regarding claim **21**, Van Der Have discloses the distribution grids form an orthogonal grid pattern (figs. 1 – 8).

Regarding claim **22**, Van Der Have discloses:

A substrate 45/57 (fig. 12) of semiconductor material;

a copper interconnection layer 46 (fig. 12; col. 26, lines 67 and 68; claims 1 and 4. (Note that claim 4 states the conducive layers are formed of metals taken from the group consisting of aluminum, copper and gold, therefore, layer 46 is formed of copper)) overlying the substrate;

an insulator layer 55 (fig. 12) overlying the metalization layer and including a plurality of vias 50 (fig. 12; col. 26, lines 64 – 68);

an aluminum distribution layer47 (fig. 12; col. 26, lines 67 and 68; claims 1 and 4; **not 48** as argued by the Applicants. (Note that claim 4 states the conducive layers are formed of metals taken from the group consisting of aluminum, copper and gold, therefore, layer 47 is formed of aluminum)) overlying the insulator layer and making selective contact with the copper interconnection layer through the vias, the aluminum distribution layer including wire bonding pads 52 (fig. 12; col. 27, lines 12 - 25) and distribution grids (figs. 1 – 8) for distributing a signal over a region of the interconnection layer, the distribution grids coupled bonding pads and distributed over the insulator layer.

Van Der Have d oes not explicitly show a package supporting the substrate and including ground and power bonding pads wire bonded to the wire bonding pads.

However, it is known that PCB or other means of substrate being provided for supporting the IC die substrate and including ground and power bonding pads wire bonded to the wire bonding pads as shown by Lee (fig. 12; [0014] – [0021]; Note: PCB is known to include power, ground, and signal layer, therefore, it is inherent that Lee's PCB would have ground, power and pads as claimed).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a PCB as a package supporting into the IC of Van Der Have as shown by Lee, in order to mount more than one IC die inside the package ([0016]) for making MCM and MCP products.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

February 07, 2006